METHOD OF DETERMINING DC MARGIN OF A LATCH

Technical Field

The invention relates to electronic circuits. More particularly, the invention relates to simulation and determination of design parameters of an electronic circuit.

Background Art

A latch is a circuit element that maintains a particular state between state changing events, i.e., in response to a particular input, and is ubiquitous in digital sequential circuit designs. For example, as shown in Fig. 1, a typical latch **100** may include, inter alia, a forward inverter **101**, a feedback inverter **102**, an input terminal **103** and an output terminal **104**. The output voltage level, V_{OUT}, remains at a particular voltage level, i.e., either high or low, until an input signal, V_{IN}, is received at the input terminal **103**, at which time the state of the output may change depending on the nature of the input signal. For example, the state of the output **104** may change from a high state to a low state upon receipt of a logical high signal at the input **103**.

In order for the latch to operate properly, i.e., to change state upon receiving a particular input, the input signal levels to the latch must exceed certain thresholds with a sufficient margin. To this end, during a circuit design, it must be ensured that the input signal levels delivered through various signal paths to each of latches in the circuit under design meet the above input signal margin.

One of the ways to ensure satisfaction of the above input signal level requirement is to determine what is often referred to as the "DC margin" for each of the latches present in the circuit being designed.

The DC margin is a pair of values, the one margin and the zero margin. The one margin is the difference between the trip voltage (V_{trip}) of the forward inverter **101** of the latch **100** and the worst case pull-up input signal level that may be presented to the latch. The zero margin is the difference between the V_{trip} of the forward inverter **101** and the worst case pull-down input signal level that may be presented to the latch **100**. The trip voltage V_{trip} is defined as the equilibrium voltage level of the output voltage level and the input voltage level of the forward inverter. In order for a particular circuit design to be deemed acceptable, the DC margin must exceed a minimum margin according to a design guideline.

Unfortunately, heretofore, in order to determine the DC margin of a latch, every possible signal paths from each of the possible circuit elements that may drive the latch must be examined, requiring performance of simulations, using a simulation program, e.g., the SPICE™, for each of the possible signal paths. The prior attempts to determine the DC margin requires numerous simulations, each of which takes a long time to perform, and are thus inefficient and time consuming. This problem may be exacerbated if there are numerous latches in the particular circuit under design.

Thus, there is a need for more efficient method of determining DC margin of a latch, which does not require numerous simulations for every possible signal paths to the latch.

Summary of Invention

In accordance with the principles of the present invention, a method of determining a DC margin of a latch comprises performing a first simulation using a first simulation circuit to determine a trip voltage of a forward inverter of the latch, performing a second simulation using a second simulation circuit to determine a one margin of the latch, the second simulation circuit comprising a worst case pull-up signal path, and performing a third simulation using a third simulation circuit to determine a zero margin of the latch, the third simulation circuit comprising a worst case pull-down signal path .

In accordance with another aspect of the principles of the present invention, a computer program stored on a computer readable storage medium implements a method of determining a DC margin of a latch, and comprises a set of instructions for performing a first simulation using a first simulation circuit to determine a trip voltage of a forward inverter of the latch, performing a second simulation using a second simulation circuit to determine a one margin of the latch, the second simulation

circuit comprising a worst case pull-up signal path, and performing a third simulation using a third simulation circuit to determine a zero margin of the latch, the third simulation circuit comprising a worst case pull-down signal path .

In yet another aspect of the principles of the present invention, a simulation circuit for determining a DC margin of a latch comprises a latch portion representing the latch being simulated, the latch portion comprising a forward inverter and a feedback inverter, an input of the forward inverter being operably connected to an input of the latch portion, and an input of the feedback inverter being operably connected to an output of the latch portion, a driver portion representing a driver circuit element capable of supplying an input signal to the latch being simulated, and a pass path subcircuit configured to receive a drive signal from the driver portion, and configured to supply the drive signal to the input of the latch portion, the pass path subcircuit representing one or more pass circuit elements along a worst case signal path between the driver circuit element and the latch being simulated.

Description of Drawings

Features and advantages of the present invention will become apparent to those skilled in the art from the following description with reference to the drawings, in which:

Figure 1 is a logic diagram of showing the relevant portions of a conventional latch.

Figure 2 is a circuit diagram illustrative of an embodiment of a simulation model circuit of the a latch and the corresponding input signal path to the latch in accordance with the principles of the present invention;

Figure 2A is a circuit diagram illustrative of an embodiment of the path subcircuit shown in Fig. 2;

Figure 3 is flow diagram illustrative of an exemplary embodiment of the process of determining the DC margin of a latch in accordance with an embodiment of the principles of the present invention;

Figure 4 is a circuit diagram illustrative of an embodiment of a simulation circuit for determining the trip voltage of a forward inverter of a latch in accordance with the principles of the present invention;

Figure 5 is a circuit diagram illustrative of an embodiment of a simulation circuit for determining the one margin of a latch in accordance with the principles of the present invention; and

Figure 6 is a circuit diagram illustrative of an embodiment of a simulation circuit for determining the zero margin of a latch in accordance with the principles of the present invention.

Detailed Description of Preferred Embodiments

For simplicity and illustrative purposes, the principles of the present invention are described by referring mainly to an exemplar embodiment, particularly, with a specific exemplary implementations of various simulation circuits. However, one of ordinary skill in the art would readily recognize that the same principles are equally applicable to, and can be implemented in, other implementations and designs using any other equivalent simulation circuits, and that any such variation would be within such modifications that do not depart from the true spirit and scope of the present invention.

In accordance with the principles of the present invention, a DC margin of a latch of a circuit under design is determined by performing three simulations. A simulation is performed to find the trip voltage of the forwarding inverter of the latch. A second simulation is performed to find the one margin of the latch. Lastly, a third simulation is performed to find the zero margin of the latch.

During each of the simulations to find the one margin and the zero margin, the worst case input signal path from the various driver circuit elements and signal paths within the circuit under design is determined analytically by accumulating weighted resistance of each of the circuit elements along the signal paths. The weights assigned to the circuit elements are empirically determined based on the topology configuration of each of the circuit elements, e.g., the type circuit element, the signal being passed through the circuit element and whether a threshold voltage drop occurs between the drive circuit element and the pass circuit element.

In particular, Fig. 2 shows a simulation model circuit **200** representing a latch and its input signal path in accordance with an embodiment of the present invention. The simulation model circuit represents an equivalent circuit model of the actual circuit being simulated, and may not include every circuit elements present in the actual circuit being simulated. For example, the NFET Q1 **201** may represent more than one circuit element, e.g., a series of NFETs, of the actual circuit being simulated.

It should be understood by those familiar with circuit evaluation techniques that each of circuit elements shown in the model circuit **200** shown in Fig. 2 may be an equivalent circuit of, and represent, a number of circuit elements of the actual circuit under simulation.

The simulation model circuit comprises a latch model **100'**, which includes two complementary field effect transistor (FET) pairs, each representing the forward inverter and the feedback inverter of the latch. The complementary pair Q1 **201** and Q2 **202** together represent the forward inverter while the complementary pair Q3 **203** and Q4 **204** represent the feedback inverter.

The model circuit **200** further comprises a path subcircuit **207** which represent the various circuit elements along a signal path between the input **103** of the latch and a circuit element that may drive the input of the latch. The circuit element that drives the input of the latch is represented by the FETs Q5 **205** and Q6 **206**, each providing a pull-down input signal and a pull-up input signal, respectively, to the input of the latch (i.e., Vin **103**) through the path subcircuit **207**. As shown, when a logical low signal V_{INH} **208** is supplied to the gate of the PFET Q6 **206**, the PFET Q6 **206** is turned on, and thus Vin **103** is driven high. When a logical high signal V_{INL} **208** is supplied to the gate of the NFET Q5 **205**, the PFET Q5 **205** is turned on, and thus Vin **103** is driven low.

Fig. 2A shows the path subcircuit **207** in more detail. According to an embodiment of the present invention, the path subcircuit **207** comprises n/2 complementary pairs of FETs, Q_{S1} to Q_{Sn}, each of which can be configured to have variable size, and can be individually removed from the path subcircuit **207**, to simulate the worst case pull-up and pull-down signal paths. In a preferred embodiment of the present invention, the path subcircuit **207** comprises six (6) complementary pairs of FETs.

In an embodiment of the present invention, the worst case pull-up and pull-down signal paths are determined analytically by traversing through each of possible signal paths from the input of the latch to each of circuit elements that can drive the input of the latch, and identifying pass circuit elements along each of the signal paths, through which a signal may pass. For each of identified pass circuit elements, a weight is applied to its resistance, e.g., based on its length and width (L/W). The weights applied to the resistance of the pass circuit elements are empirically determined based on the topology configuration of each of the circuit elements, e.g., the pass circuit element type (e.g., whether the pass

circuit element is a single NFET, single PFET or a complementary pair of FETs), the signal being passed through the pass circuit element and whether a threshold voltage drop occurs between the drive circuit element and the pass circuit element.

The weighted resistance of the identified pass circuit elements along a particular signal path are added together to determine the total resistance of the particular signal path, and is compared to the total resistance similarly calculated for other signal paths to determine the worst case signal path which results in the worst degradation of signal level while passing through the signal path.

In a preferred embodiment of the present invention, the path subcircuit **207** is configured to include one or more of the FETs, Q_{S1} and Q_{Sn}, each included FET representing identified pass circuit elements. The sizes of the included FETs in the path subcircuit **207** are based on the sizes of the respective pass circuit elements. In an alternative embodiment, the path subcircuit **207** may simply be a resistor element having the weighted total resistance of the worst case signal path identified.

The inventive process of determining DC margin of a latch will now be described with references to FIGs. 4 through 6. In step **301**, a simulation, e.g., using SPICE™ which is known to those familiar with circuit design testing, is performed to determine the trip point voltage (V_{trip}) of the forward inverter of the latch. An exemplary embodiment of the simulation circuit **400** for the V_{trip} determination is shown in Fig. 4. In this example, the simulation circuit **400** includes the forward inverter portion of the latch, and comprises the complementary pair of FETs, Q1 **201** and Q2 **202**.

As shown, in the simulation circuit **400**, the input terminal Vin **103** and the output terminal Vout **104** of the forward inverter are connected together. The simulation comprises a DC analysis of the simulation circuit **400** to determine the settling voltage level at the input terminal Vin **103**, which is the same as the voltage level at the output terminal Vout **104**. Once the voltage levels at the input terminal and the output terminal settles to equal each other, th settling voltage is the trip point voltage (V_{trip}) of the forward inverter of the latch.

In step **302**, the worst case pull-up signal path and the path subcircuit **207** based on the worst case pull-up signal path are found as previously described. In particular, in an embodiment of the present invention, the worst case pull-up signal path is determined analytically by traversing through each of possible signal paths from the input of the latch to each of pull-up driver circuit elements that

can drive a pull-up signal to the input of the latch, and identifying pass circuit elements along each of the signal paths, through which a signal may pass. For each of identified pass circuit elements, a weight is applied to its resistance, e.g., based on its length and width (L/W). The weights applied to the resistance of the pass circuit elements are empirically determined based on the topology configuration of each of the circuit elements, e.g., the pass circuit element type (e.g., whether the pass circuit element is a single NFET, single PFET or a complementary pair of FETs), the signal being passed through the pass circuit element and whether a threshold voltage drop occurs between the pull-up driver circuit element and the pass circuit element.

The weighted resistance of the identified pass circuit elements along a particular signal path are added together to determine a cumulative resistance of the particular signal path, i.e., from the supply voltage V_{DD} through the pull-up driver circuit element and the pass circuit elements to the latch input. The cumulative resistence of each signal path is compared to the total resistance similarly calculated for other signal paths to determine the worst case pull-up signal path, i.e., the signal path with the highest cumulative resistance, which results in the worst degradation of signal level while passing through the signal path.

The pull-up driver of the identified worst case pull-up signal path is mapped to an equivalent canonical driver circuit Q6 **206** as shown in Fig. 5. The path subcircuit **207a** is constructed to include one or more of the FETs, Q_{S1} and Q_{Sn} (as shown in Fig. 2A), each included FET representing identified pass circuit elements of the worst case pull-up signal path. The sizes of the FETs included in the path subcircuit **207** are based on the sizes of the respective pass circuit elements.

In step **303**, a simulation is performed to determine the one margin ($Vmar_{(1)}$). An exemplary embodiment of the simulation circuit **500** for the $Vmar_{(1)}$ determination is shown in Fig. 5. The $Vmar_{(1)}$ simulation circuit **500** includes the forward inverter portion, i.e., the complementary pair of FETs Q1 and Q2, the NFET Q3, the PFET Q6 and the path subcircuit **207a** constructed in step **302** above. In this exemplary simulation circuit **500**, the FETs Q4 **204** and Q5 **205** shown in Fig. 2 are omitted. However, in an alternative embodiment, the FETs Q4 **204** and Q5 **205** may be included, and turned off.

The $Vmar_{(1)}$ simulation comprises a DC analysis of the simulation circuit **500** with the output Vout **104** initially set to logical high, i.e., set to V_{DD}, and determining the voltage level at the input terminal Vin **103**. If the voltage level at the input terminal Vin **103** exceeds the V_{trip}, and is sufficiently high to overcome the NFET Q3 **203**, the state of the output, Vout **104**, would switch from the high initial setting to a logical low. The one margin, $Vmar_{(1)}$, is the difference of the voltage level at Vin **103** and V_{trip}, i.e., $Vmar_{(1)} = Vin - V_{trip}$.

In step **304**, the worst case pull-down signal path and the path subcircuit **207** based on the worst case pull-down signal path are found as previously described. In particular, in an embodiment of the present invention, the worst case pull-down signal path is determined analytically by traversing through each of possible signal paths from the input of the latch to each of pull-down driver circuit elements that can drive a pull-down signal to the input of the latch, and identifying pass circuit elements along each of the signal paths, through which the pull-down signals may pass. For each of identified pass circuit elements, a weight is applied to its resistance, e.g., based on its length and width (L/W). The weights applied to the resistance of the pass circuit elements are empirically determined based on the topology configuration of each of the circuit elements, e.g., the pass circuit element type (e.g., whether the pass circuit element is a single NFET, single PFET or a complementary pair of FETs), the signal being passed through the pass circuit element and whether a threshold voltage drop occurs between the pull-down driver circuit element and the pass circuit element.

The weighted resistance of the identified pass circuit elements along a particular signal path are added together to determine a cumulative resistance of the particular signal path, i.e., from the ground (GND) through the pull-down driver circuit element and the pass circuit elements to the latch input. The cumulative resistence of each signal path is compared to the total resistance similarly calculated for other pull-down signal paths to determine the worst case pull-down signal path, i.e., the signal path with the highest cumulative resistance.

The pull-down driver of the identified worst case pull-down signal path is mapped to an equivalent canonical driver circuit Q5 **206** as shown in Fig. 5. The path subcircuit **207b** is constructed to include one or more of the FETs, Q_{S1} and Q_{Sn} (as shown in Fig. 2A), each included FET representing identified pass circuit elements of the worst case pull-down signal path. The sizes of the

FETs included in the path subcircuit **207** are based on the sizes of the respective pass circuit elements.

In step **305**, a simulation is performed to determine the zero margin ($Vmar_{(0)}$). An exemplary embodiment of the simulation circuit **600** for the $Vmar_{(0)}$ determination is shown in Fig. 6. The $Vmar_{(0)}$ simulation circuit **600** includes the forward inverter portion, i.e., the complementary pair of FETs Q1 and Q2, the NFET Q5, the PFET Q4 and the path subcircuit **207b** constructed in step **304** above. In this exemplary simulation circuit **600**, the FETs Q3 **203** and Q6 **206** shown in Fig. 2 are omitted. However, in an alternative embodiment, the FETs Q3 **203** and Q6 **206** may be included, and turned off.

The $Vmar_{(0)}$ simulation comprises a DC analysis of the simulation circuit **600** with the output Vout **104** initially set to logical low, i.e., set to ground, and determining the voltage level at the input terminal Vin **103**. If the voltage level at the input terminal Vin **103** is below the V_{trip}, and is sufficiently low to overcome the PFET Q4 **204**, the state of the output, Vout **104**, would switch from the low initial setting to a logical high. The zero margin, $Vmar_{(0)}$, is the difference of V_{trip} and the voltage level at Vin **103**, i.e., $Vmar_{(0)} = V_{trip}$ - Vin. Finally, the process ends in step **306**.

If each of the one margin and the zero margin exceed a design guideline margin thresholds, the circuit design is deemed acceptable, and proper operations of the latch is ensured.

As can be appreciated, the DC margin determination method described herein allows an efficient and fast determination of DC margin of a latch without requiring numerous time consuming simulations for each of the possible signal paths to the input of the latch.

Specific program listings for an embodiment of a method of determining the DC margin of a latch in accordance with the principles of the present invention is provided in the Appendix, which appears below.

While the invention has been described with reference to the exemplary embodiments thereof, those skilled in the art will be able to make various modifications to the described embodiments of the invention without departing from the true spirit and scope of the invention. The terms and descriptions used herein are set forth by way of illustration only and are not meant as limitations. In particular, although the method of the present invention has been described by examples, the steps of the method may be performed in a different order than illustrated or simultaneously. Those skilled in the art will

recognize that these and other variations are possible within the spirit and scope of the invention as defined in the following claims and their equivalents.